



Arm[®] Cortex[®]-A320 Core Cryptographic Extension

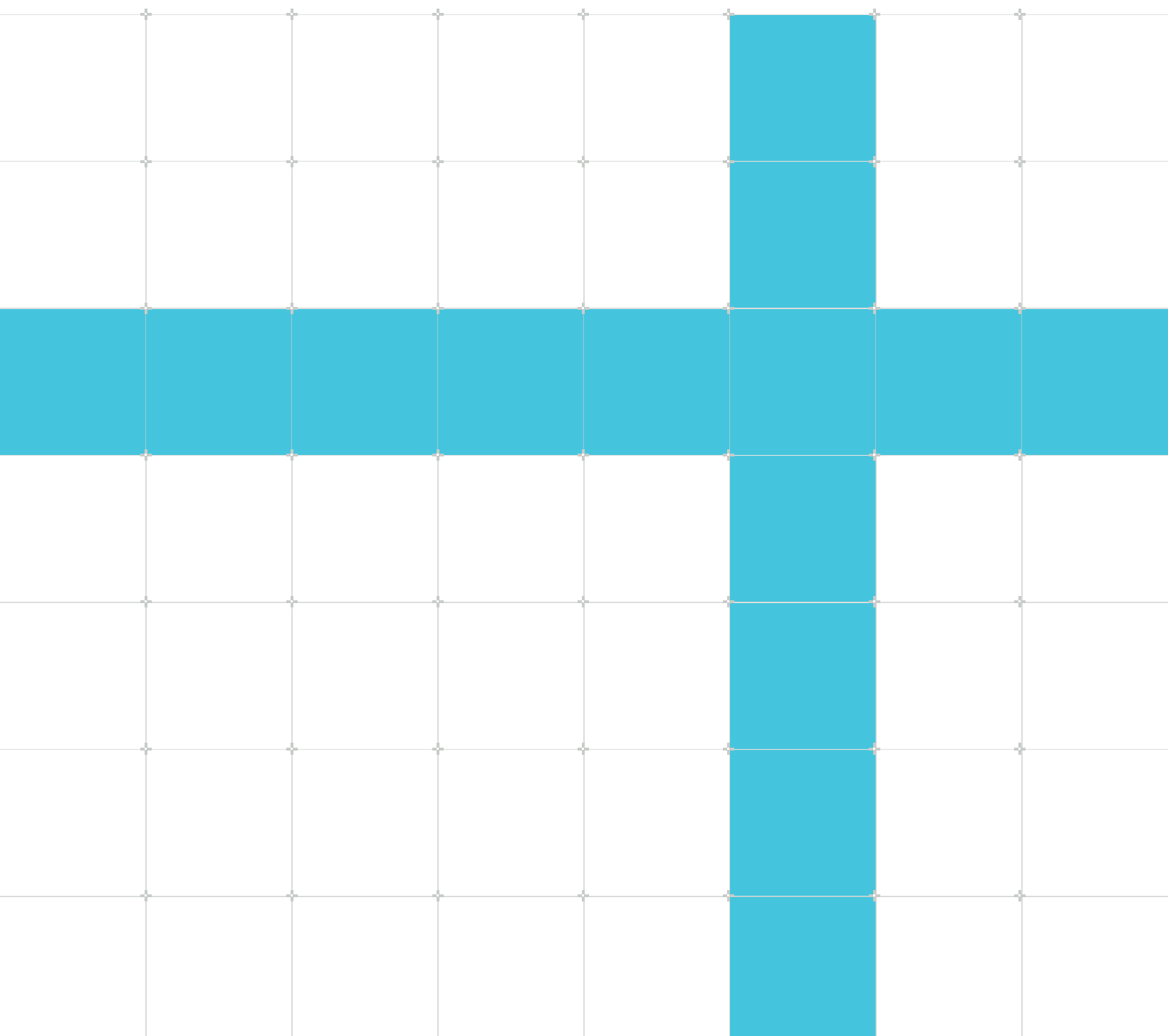
Revision r0p1

Technical Reference Manual

Non-Confidential

Issue 03

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Arm® Cortex®-A320 Core Cryptographic Extension Technical Reference Manual

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This document (109553_0001_03_en) was issued on 2025-04-04. There might be a later issue at <https://developer.arm.com/documentation/109553>

The product revision is r0p1.

See also: [Proprietary Notice](#) | [Product and document information](#) | [Useful resources](#)

Start reading

If you prefer, you can skip to [the start of the content](#).

Intended audience

This manual is for system designers, system integrators, and programmers who are designing or programming a *System-on-Chip* (SoC) that uses the Cortex®-A320 core with the optional Cryptographic Extension.

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1. Cryptographic Extension support in the Cortex®-A320 core

The Cortex®-A320 core supports the optional Arm® Cryptographic Extension.

The Arm® Cryptographic Extension adds A64 instructions to Advanced SIMD to:

- Accelerate *Advanced Encryption Standard* (AES) encryption and decryption
- Implement the *Secure Hash Algorithm* (SHA) functions
- Perform *Polynomial Multiply Long* (PMULL) instructions

Supported features

The Arm® Cryptographic Extension supports the following features:

Table 1-1: Features supported by the Arm® Cryptographic Extension

Feature	Description	Architecture version
FEAT_AES	Advanced SIMD AES instructions	Arm®v8.0
FEAT_PMULL	Advanced SIMD PMULL instructions	
FEAT_SHA1	Advanced SIMD SHA1 instructions	
FEAT_SHA256	Advanced SIMD SHA256 instructions	
FEAT_SHA512	Advanced SIMD SHA512 instructions	Arm®v8.2
FEAT_SHA3	Advanced SIMD EOR3, RAX1, XAR, and BCAX instructions	
FEAT_SM3	Advanced SIMD SM3 instructions	
FEAT_SM4	Advanced SIMD SM4 instructions	
FEAT_SVE_AES	SVE AES instructions	Arm®v9.0
FEAT_SVE_PMULL128	SVE PMULL instructions	
FEAT_SVE_SHA3	SVE SHA3 instructions	
FEAT_SVE_SM4	SVE SM4 instructions	

1.1 Disabling the Cryptographic Extension

Disabling the Cryptographic Extension applies to all Cortex®-A320 cores in a cluster.

To disable the Cryptographic Extension, assert the CRYPTODISABLE signal.

When the CRYPTODISABLE signal is asserted:

- Executing a cryptographic instruction results in an **UNDEFINED** exception.
- ID_AA64ISAR0_EL1 and ID_AA64ZFR0_EL1 indicate that the Cryptographic Extension is not implemented.

Related information

- 2.2 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0 on page 6
- 2.3 ID_AA64ZFR0_EL1, SVE Feature ID Register 0 on page 10

1.2 Product revisions

The following table indicates the main differences in functionality between product revisions.

Table 1-2: Product revisions

Revision	Notes
r0p0	First release
r0p1	Bug fixes and performance improvements. For more information about bug fixes, see the Cortex®-A320 core Software Developer's Errata Notice or the Cortex®-A320 core Product Errata Notice.

Changes in functionality that have an impact on the documentation also appear in [Revision history](#) on page 16.

2. AArch64 instruction identification system registers

This chapter describes the ID_AA64ISAR0_EL1 and ID_AA64ZFR0_EL1 registers. These identification registers provide information about the instructions implemented in the Cortex®-A320 core, including the instructions provided by the Cryptographic Extension.

2.1 Cryptographic Extensions register summary

The Cortex®-A320 core has a single instruction identification register, ID_AA64ISAR0_EL1. Software can identify the cryptographic instructions that are implemented by reading this register.

The following table shows the instruction identification register for the Cortex®-A320 core Cryptographic Extension.

Table 2-1: Cryptographic Extension register summary

Name	Description
ID_AA64ISAR0_EL1	See 2.2 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0 on page 6
ID_AA64ZFR0_EL1	See 2.3 ID_AA64ZFR0_EL1, SVE Feature ID Register 0 on page 10

2.2 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0

Provides information about the instructions implemented in AArch64 state.

For general information about the interpretation of the ID registers, see *Principles of the ID scheme for fields in ID registers* in the [Arm® Architecture Reference Manual for A-profile architecture](#).

Configurations

This register is available in all configurations.

Attributes

Width

64

Functional group

Identification registers

Access type

RO

Reset value

xxxx	0010	0010	0001	0001	xxxx	xxxx	xxxx	0001	0000	0010	0001	xxxx	xxxx	xxxx	xxxx
63	59	55	51	47	43	39	35	31	27	23	19	15	11	7	3
															0



Where the reset reads xxxx, see individual bits.

Bit descriptions

Figure 2-1: AARCH64_ID_AA64ISAR0_EL1 bit assignments

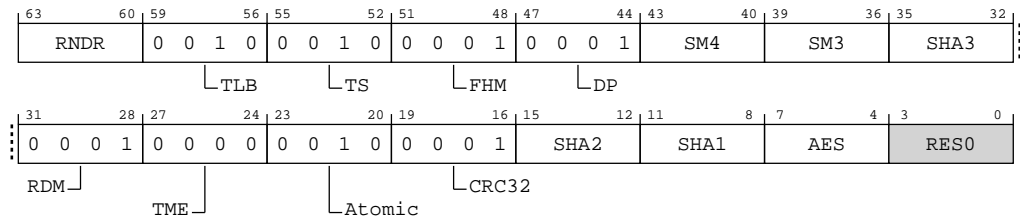


Table 2-2: ID_AA64ISAR0_EL1 bit descriptions

Bits	Name	Description	Reset
[63:60]	RNDR	Indicates support for Random Number instructions in AArch64 state. When FEAT_RNG_TRAP is implemented, the value returned by a direct read of ID_AA64ISAR0_EL1.RNDR is further controlled by the value of SCR_EL3.TRNDR. 0b0000 No Random Number instructions are implemented. 0b0001 RNDR and RNDRRS registers are implemented.	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[59:56]	TLB	Indicates support for Outer Shareable and TLB range maintenance instructions. 0b0010 Outer Shareable and TLB range maintenance instructions are implemented.	0b0010
[55:52]	TS	Indicates support for flag manipulation instructions. 0b0010 CFINV, RMIF, SETF16, SETF8, AXFLAG, and XAFLAG instructions are implemented.	0b0010
[51:48]	FHM	Indicates support for FMLAL and FMLSL instructions. 0b0001 FMLAL and FMLSL instructions are implemented.	0b0001

Bits	Name	Description	Reset
[47:44]	DP	Indicates support for Dot Product instructions in AArch64 state. 0b0001 UDOT and SDOT instructions implemented.	0b0001
[43:40]	SM4	Indicates support for SM4 instructions in AArch64 state. 0b0000 No SM4 instructions implemented. This value applies when the complex is not implemented with the Cryptographic Extensions or the CRYPTODISABLE input is HIGH. 0b0001 SM4E and SM4EKEY instructions implemented. This value applies when the complex is implemented with the Cryptographic Extensions and the CRYPTODISABLE input is LOW.	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[39:36]	SM3	Indicates support for the following SM3 instructions SM3SS1, SM3TT1A, SM3TT1B, SM3TT2A, SM3TT2B, SM3PARTW1, and SM3PARTW2 in AArch64 state. 0b0000 The specified instructions are not implemented. This value applies when the complex is not implemented with the Cryptographic Extensions or the CRYPTODISABLE input is HIGH. 0b0001 The specified instructions are implemented. This value applies when the complex is implemented with the Cryptographic Extensions and the CRYPTODISABLE input is LOW.	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[35:32]	SHA3	Indicates support for the following SHA3 instructions EOR3, RAX1, XAR, and BCAX in AArch64 state. 0b0000 The specified instructions are not implemented. This value applies when the complex is not implemented with the Cryptographic Extensions or the CRYPTODISABLE input is HIGH. 0b0001 The specified instructions are implemented. This value applies when the complex is implemented with the Cryptographic Extensions and the CRYPTODISABLE input is LOW.	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[31:28]	RDM	Indicates support for SQRDMLAH and SQRDMLSH instructions in AArch64 state. 0b0001 SQRDMLAH and SQRDMLSH instructions implemented.	0b0001
[27:24]	TME	Indicates support for the following TME instructions TCANCEL, TCOMMIT, TSTART, and TTEST. 0b0000 The specified instructions are not implemented. Access to this field is: RO	0b0000

Bits	Name	Description	Reset
[23:20]	Atomic	Indicates support for Atomic instructions in AArch64 state. 0b0010 LDADD, LDCLR, LDEOR, LDSET, LDSMAX, LDSMIN, LDUMAX, LDUMIN, CAS, CASP, and SWP instructions implemented.	0b0010
[19:16]	CRC32	Indicates support for the following CRC32 instructions CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, and CRC32CX in AArch64 state. 0b0001 The specified instructions are implemented.	0b0001
[15:12]	SHA2	Indicates support for SHA2 instructions in AArch64 state. 0b0000 No SHA2 instructions implemented. This value applies when the complex is not implemented with the Cryptographic Extensions or the CRYPTODISABLE input is HIGH. 0b0010 Implements instructions: <ul style="list-style-type: none"> SHA256H, SHA256H2, SHA256SU0, and SHA256SU1. SHA512H, SHA512H2, SHA512SU0, and SHA512SU1. This value applies when the complex is implemented with the Cryptographic Extensions and the CRYPTODISABLE input is LOW.	The reset values can be the following: 0b0000, 0b0010, respective to the value.
[11:8]	SHA1	Indicates support for the following SHA1 instructions SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 in AArch64 state. 0b0000 The specified instructions are not implemented. This value applies when the complex is not implemented with the Cryptographic Extensions or the CRYPTODISABLE input is HIGH. 0b0001 The specified instructions are implemented. This value applies when the complex is implemented with the Cryptographic Extensions and the CRYPTODISABLE input is LOW.	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[7:4]	AES	Indicates support for AES instructions in AArch64 state. 0b0000 No AES instructions implemented. This value applies when the complex is not implemented with the Cryptographic Extensions or the CRYPTODISABLE input is HIGH. 0b0010 AESE, AESD, AESMC, and AESIMC instructions implemented, and PMULL and PMULL2 instructions operating on 64-bit source elements. This value applies when the complex is implemented with the Cryptographic Extensions and the CRYPTODISABLE input is LOW.	The reset values can be the following: 0b0000, 0b0010, respective to the value.
[3:0]	RES0	Reserved	RES0

Access

MRS <Xt>, ID_AA64ISAR0_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0110	0b000

Accessibility

MRS <Xt>, ID_AA64ISAR0_EL1

```

if PSTATE.EL == EL0 then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
elseif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = ID_AA64ISAR0_EL1;
elseif PSTATE.EL == EL2 then
    X[t, 64] = ID_AA64ISAR0_EL1;
elseif PSTATE.EL == EL3 then
    X[t, 64] = ID_AA64ISAR0_EL1;

```

2.3 ID_AA64ZFR0_EL1, SVE Feature ID Register 0

Provides additional information about the implemented features of the AArch64 Scalable Vector Extension, when FEAT_SVE is implemented.

For general information about the interpretation of the ID registers, see *Principles of the ID scheme for fields in ID registers* in the [Arm® Architecture Reference Manual for A-profile architecture](#).

Configurations



Note

Prior to the introduction of the features described by this register, this register was unnamed and reserved, **RES0** from EL1, EL2, and EL3.

If FEAT_SME is implemented and FEAT_SVE is not implemented, then SVE instructions can only be executed when the PE is in Streaming SVE mode and the instructions are legal to execute in Streaming SVE mode.

Attributes

Width

64

Functional group

Identification registers

Access type

RO

Reset value

xxxx	0000	0000	xxxx	0001	xxxx	xxxx	xxxx	xxxx	xxxx	0001	0001	xxxx	xxxx	xxxx	0001
63	59	55	51	47	43	39	35	31	27	23	19	15	11	7	3



Where the reset reads xxxx, see individual bits.

Bit descriptions

Figure 2-2: AARCH64_ID_AA64ZFR0_EL1 bit assignments



Table 2-4: ID_AA64ZFR0_EL1 bit descriptions

Bits	Name	Description	Reset
[63:60]	RES0	Reserved	RES0
[59:56]	F64MM	Indicates support for the following SVE FP64 double-precision variant of the FMMLA instruction, the LD1RO* instructions, the 128-bit element variants of the SVE TRN1 , TRN2 , UZP1 , UZP2 , ZIP1 , and ZIP2 instructions. 0b0000 Double-precision matrix multiplication and related SVE instructions are not implemented.	0b0000
[55:52]	F32MM	Indicates support for the SVE FP32 single-precision floating-point matrix multiplication instruction. 0b0000 Single-precision matrix multiplication instruction is not implemented.	0b0000
[51:48]	RES0	Reserved	RES0
[47:44]	I8MM	Indicates support for the following SVE Int8 matrix multiplication instructions SVE SMMLA , SUDOT , UMMLA , USMMLA , and USDOT . 0b0001 The specified instructions are implemented.	0b0001

Bits	Name	Description	Reset
[43:40]	SM4	<p>Indicates support for SVE SM4 instructions.</p> <p>0b0000 SVE SM4 instructions are not implemented.</p> <p>This value applies when the complex is not implemented with the Cryptographic Extensions or the CRYPTODISABLE input is HIGH.</p> <p>0b0001 SVE SM4E and SM4EKEY instructions are implemented.</p> <p>This value applies when the complex is implemented with the Cryptographic Extensions and the CRYPTODISABLE input is LOW.</p>	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[39:36]	RES0	Reserved	RES0
[35:32]	SHA3	<p>Indicates support for the SVE SHA3 instructions.</p> <p>0b0000 SVE SHA3 instructions are not implemented.</p> <p>This value applies when the complex is not implemented with the Cryptographic Extensions or the CRYPTODISABLE input is HIGH.</p> <p>0b0001 SVE RAX1 instruction is implemented.</p> <p>This value applies when the complex is implemented with the Cryptographic Extensions and the CRYPTODISABLE input is LOW.</p>	The reset values can be the following: 0b0000, 0b0001, respective to the value.
[31:24]	RES0	Reserved	RES0
[23:20]	BF16	<p>Indicates support for SVE BFloat16 instructions.</p> <p>0b0001 SVE BFCVT, BFCVTNT, BFDOT, BFMLALB, BFMLALT, and BFMLLA instructions are implemented.</p>	0b0001
[19:16]	BitPerm	<p>Indicates support for the following SVE bit permute instructions SVE BDEP, BEXT, and BGRP.</p> <p>0b0001 The specified instructions are implemented.</p>	0b0001
[15:8]	RES0	Reserved	RES0
[7:4]	AES	<p>Indicates support for SVE AES instructions.</p> <p>0b0000 SVE AES* instructions are not implemented.</p> <p>This value applies when the complex is not implemented with the Cryptographic Extensions or the CRYPTODISABLE input is HIGH.</p> <p>0b0010 SVE AESE, AESD, AESMC, AESIMC, and 64-bit source element variants of SVE PMULLB and PMULLT instructions are implemented.</p> <p>This value applies when the complex is implemented with the Cryptographic Extensions and the CRYPTODISABLE input is LOW.</p>	The reset values can be the following: 0b0000, 0b0010, respective to the value.

Bits	Name	Description	Reset
[3:0]	SVEver	Indicates support for SVE instructions when FEAT_SME or FEAT_SVE is implemented. 0b0001 The SVE instructions and the mandatory SVE2 instructions are implemented.	0b0001

Access

MRS <Xt>, ID_AA64ZFR0_EL1

op0	op1	CRn	CRm	op2
0b11	0b000	0b0000	0b0100	0b100

Accessibility

MRS <Xt>, ID_AA64ZFR0_EL1

```
if PSTATE.EL == EL0 then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
elseif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        X[t, 64] = ID_AA64ZFR0_EL1;
elseif PSTATE.EL == EL2 then
    X[t, 64] = ID_AA64ZFR0_EL1;
elseif PSTATE.EL == EL3 then
    X[t, 64] = ID_AA64ZFR0_EL1;
```

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110 Fulbourn Road, Cambridge, England CB1 9NJ.

PRE-1121-V1.0

Product and document information

Read the information in these sections to understand the release status of the product and documentation, and the conventions used in the Arm documents.

Product status

All products and Services provided by Arm require deliverables to be prepared and made available at different levels of completeness. The information in this document indicates the appropriate level of completeness for the associated deliverables.

Product completeness status

The information in this document is Final, that is for a developed product.

Product revision status

This product is r0p1, which indicates the revision status of the product described in this manual, where:

- r (value)** Identifies the major revision of the product, for example, r1.
- p (value)** Identifies the minor revision or modification status of the product, for example, p2.

Revision history

These sections can help you understand how the document has changed over time.

Document release information

The Document history table gives the issue number and the released date for each released issue of this document.

Document history

Issue	Date	Confidentiality	Change
0001-03	4 April 2025	Non-Confidential	First release for r0p1
0000-02	26 February 2025	Non-Confidential	Second early access release for r0p0
0000-01	6 December 2024	Confidential	First early access release for r0p0

The Change history tables describe the technical changes between released issues of this document in reverse order. Issue numbers match the revision history in [Document release information](#) on page 16.

Table 2: Issue 0000-01

Change	Location
First early access release for r0p0	-

Table 3: Differences between issue 0000-01 and issue 0000-02

Change	Location
Second early access release for r0p0	-
Editorial changes	Throughout the document
Updated product name	Throughout the document

Table 4: Differences between issue 0000-02 and issue 0001-03

Change	Location
First release for r0p1	-
Various clarifications to register	2.2 ID_AA64ISAR0_EL1, AArch64 Instruction Set Attribute Register 0 on page 6
Various clarifications to register	2.3 ID_AA64ZFR0_EL1, SVE Feature ID Register 0 on page 10

Conventions

The following subsections describe conventions used in Arm documents.

Glossary

The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm Glossary for more information: developer.arm.com/glossary.

Typographic conventions

Arm documentation uses typographical conventions to convey specific meaning.

Convention	Use
<i>italic</i>	Citations.
bold	Terms in descriptive lists, where appropriate.
monospace	Text that you can enter at the keyboard, such as commands, file and program names, and source code.
monospace <u>underline</u>	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: <pre>MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2></pre>
SMALL CAPITALS	Terms that have specific technical meanings as defined in the Arm® Glossary. For example, IMPLEMENTATION DEFINED , IMPLEMENTATION SPECIFIC , UNKNOWN , and UNPREDICTABLE .



We recommend the following. If you do not follow these recommendations your system might not work.



Your system requires the following. If you do not follow these requirements your system will not work.



You are at risk of causing permanent damage to your system or your equipment, or of harming yourself.



This information is important and needs your attention.



This information might help you perform a task in an easier, better, or faster way.



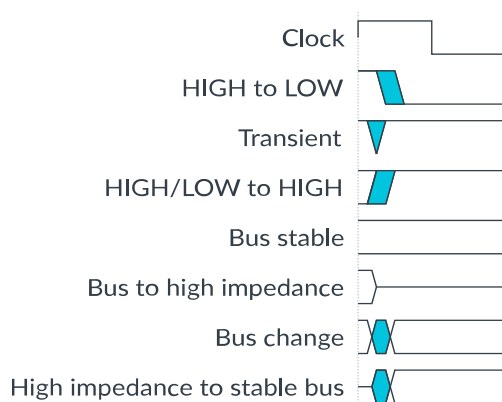
This information reminds you of something important relating to the current content.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

Figure 1: Key to timing diagram conventions



Signals

The signal conventions are:

Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name, n denotes an active-LOW signal.

Useful resources

This document contains information that is specific to this product. See the following resources for other useful information.

Arm documents are available on developer.arm.com/documentation.

Confidential documents are only available to licensees, when logged in. Each document link in the tables below provides direct access to the online version of the document.

Arm product resources	Document ID	Confidentiality
<i>Arm® Cortex®-A320 Core Configuration and Integration Manual</i>	109552	Confidential
<i>Arm® Cortex®-A320 Core Technical Reference Manual</i>	109551	Non-Confidential
Arm® Cortex®-A320 Core Release Note	110088	Confidential

Arm architecture and specifications	Document ID	Confidentiality
<i>Arm® Architecture Reference Manual for A-profile architecture</i>	DDI 0487	Non-Confidential

Non-Arm resources	Document ID	Organization
<i>Advanced Encryption Standard</i>	FIPS 197, November 2001	The National Institute of Standards and Technology (NIST) www.nist.gov
<i>Secure Hash Standard (SHS)</i>	FIPS 180-4, August 2015	The National Institute of Standards and Technology (NIST) www.nist.gov
<i>Secure Hash Standard (SHS)</i>	FIPS 202, August 2015	The National Institute of Standards and Technology (NIST) www.nist.gov